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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,677	CHA ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/05, 2/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed February 10, 2004.

Information Disclosure Statement

The non patent literature reference in the information disclosure statement filed January 14, 2005 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Objections

Claims 20, 28 and 43 are objected to because of the following informalities:

Claim 20 recites the limitation of "the exposed portions of the raised pattern". There is insufficient antecedent basis for this limitation in the claim.

In claim 28, the word "condition" should be inserted after the phrase "a second processing".

Claim 43 is unclear as written. The claim should be rewritten to clearly indicate that the oxygen gas has a flow rate of 30-150 sccm, the helium gas has a flow rate of 10-200 sccm and the silane has a flow rate of 10-100 sccm. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 41-45 and 58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 38, upon which claim 41 depends, recites the limitation of "forming a **second** insulation layer having a level surface of the first insulation layer patterns by forming a **second** insulation material" (emphasis added). However, claim 41 recites "forming the **first** insulation layer having the level surface by forming a **second** insulation material on the first insulation material". Hence, it is unclear as to whether the "second insulation material" is part of the first insulation layer or the second insulation layer.

Claim 58 does not make sense as written. Specifically, the limitations of "the second insulation layer is formed using the third insulation material by an HDP-CVD process" and "a third second processing condition substantially identical to the second processing condition" do not make sense.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5-8, 15, 16, 18-20, 22, 24-30, 35-39, 46 and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al. (US 6,204,161).

Regarding claim 1, Chung discloses a substrate (100) and a raised pattern (250/260) on the substrate, forming a first insulating layer (300) on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition and forming a second portion (300) of the first insulating layer using a second processing condition, after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate, and after removing portions of the first insulating layer, forming a second insulating layer (340/360) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (col. 7, ln. 38 – col. 8, ln. 36).

Regarding claim 3, Chung discloses that the substrate is an integrated circuit substrate, the raised pattern is a pattern of transistor gate electrodes, and maintaining portions of the first insulating layer on the substrate includes maintaining portions of the first insulating layer between transistor gate electrodes (col. 5, ln. 64 – col. 6, ln. 16).

Regarding claim 5, Chung discloses that the first insulating layer includes closed voids therein, and removing portions of the first insulating layer includes opening the voids in the first insulating layer (Fig. 4B; col. 7, ln. 60 – col. 8, ln. 7).

Regarding claims 6 and 25, Chung discloses that the openings in the voids are substantially at least as wide as portions of the opened voids between the openings and the substrate.

Regarding claims 7, 26 and 35, Chung discloses that the closed voids are located in the first insulating layer between portions of the raised pattern.

Regarding claims 8 and 27, Chung discloses that the second insulating layer fills the opened voids (col. 8, ln. 25-36).

Regarding claim 15, Chung discloses forming the first insulating layer using a high density plasma chemical vapor deposition (HDP-CVD) (col. 7, ln. 45-59).

Regarding claims 16 and 22, Chung discloses that removing portions of the first insulating layer involves etching back portions of the first insulating layer without mechanical polishing while etching back (col. 7, ln. 66 – col. 8, ln. 24).

Regarding claim 18, Chung discloses that removing portions of the first insulating layer involves removing portions of the first insulating layer beyond portions of the raised pattern so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed relative to the exposed portions of the raised pattern (Fig. 4C).

Regarding claim 19, Chung discloses that a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern before removing portions of the first insulating layer (Fig. 4B).

Regarding claim 20, Chung discloses a substrate and a raised pattern on the substrate, forming a first insulating layer (300) on the raised pattern and on the substrate such that a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern, after forming the first insulating layer, removing portions of the first insulating layer while maintaining portions of the first insulating layer so that the raised pattern extends

beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed between portions of the raised pattern, and after removing portions of the first insulating layer, forming a second insulating layer (340/360) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (col. 7, ln. 38 – col. 8, ln. 36).

Regarding claim 24, Chung discloses that the first insulating layer includes closed voids therein, and removing portions of the first insulating layer includes opening the voids in the first insulating layer (col. 8, ln. 25-36).

Regarding claim 28, Chung discloses forming a first insulation material (300) on a substrate including patterns formed thereon under a first processing condition, wherein the first insulation material has a maximum height and a void having a circular shape formed therein, and forming a first insulation layer having a level surface on the substrate including the patterns by forming a second insulation material (300) on the first insulation material under a second processing condition varied from the first processing condition, wherein the first insulation layer covering the patterns includes the voids (col. 7, ln. 38 – col. 8, ln. 36).

Regarding claims 29 and 39, Chung discloses that each of the patterns includes a gate structure (col. 5, ln. 64 – col. 6, ln. 16).

Regarding claim 30, Chung discloses that the first insulation material includes a high density plasma (HDP) oxide and the first insulation layer is formed by a high density plasma chemical vapor deposition (HDP-CVD) process (col. 7, ln. 45-59).

Regarding claim 36, Chung discloses etching the first insulation layer by an etch back process to open the void in the first insulation layer and to expose upper faces of the patterns after forming the first insulation layer (col. 7, ln. 66 – col. 8, ln. 24).

Regarding claim 37, Chung discloses forming a second insulation layer (340/360) that fills up the opened void and covers the patterns after etching the first insulation layer (col. 8, ln. 25-37).

Regarding claim 38, Chung discloses providing a substrate having patterns formed thereon, forming a first insulation layer (300) that has an level surface and covers the patterns by forming a first insulation material on the substrate, wherein voids (320) are formed at portions of the first insulation layer between the patterns, forming first insulation layer patterns between the patterns by etching the first insulation layer using an etch back process, wherein the first insulation layer patterns include widely opened voids, and forming a second insulation layer (340/360) having a level surface on the first insulation layer patterns by forming a second insulation material, wherein the second insulation layer fills up the opened void and covers the patterns (col. 7, ln. 38 – col. 8, ln. 36).

Regarding claim 46, Chung discloses that the voids have a circular shape and are positioned between the patterns.

Regarding claim 47, Chung discloses that etching the first insulation layer is performed by a wet etch process or a dry etch process (col. 8, ln. 16-18).

Claims 1-3, 15-20, 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato et al. (US 6,798,038).

Regarding claim 1, Sato discloses a substrate (1) and a raised pattern on the substrate, forming a first insulating layer (12/6/7 in Fig. 4A-4H or 6/7/26/27 in Fig. 9A-9P) on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion (12 in Fig. 4A-4H or 6/7 in Fig. 9A-9P) of the first insulating layer using a first processing condition and forming a second portion (6/7 in Fig. 4A-4H or 26/27 in Fig. 9A-9P) of the first insulating layer using a second processing condition, after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate, and after removing portions of the first insulating layer, forming a second insulating layer (8 in Fig. 4A-4H and Fig. 9A-9P) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (Fig. 4A-4H and 9A-9P; col. 6, ln. 30 – col. 7, ln. 18; col. 11, ln. 45 – col. 13, ln. 48).

Regarding claim 2, Sato discloses that the substrate is a semiconductor substrate, wherein the raised pattern is a trench isolation pattern in the semiconductor substrate and wherein maintaining portions of the first insulating layer on the substrate includes maintaining portions of the first insulating layer in trenches defined by the trench isolation pattern (Fig. 4A-4H; col. 6, ln. 30 – col. 7, ln. 18).

Regarding claim 3, Sato discloses that the substrate is an integrated circuit substrate, the raised pattern is a pattern of transistor gate electrodes, and maintaining portions of the first insulating layer on the substrate includes maintaining portions of the first insulating layer between transistor gate electrodes (Fig. 9A-9P; col. 11, ln. 45 – col. 13, ln. 48).

Regarding claim 15, Sato discloses that forming the first insulating layer (6/7 in Fig. 9A-9P) involves using a high-density plasma chemical vapor deposition (HDP-CVD) (col. 12, ln. 18-20).

Regarding claims 16 and 22, Sato discloses removing portions of the first insulating layer by etching back portions of the first insulating layer without mechanical polishing while etching back (col. 4, ln. 42-55; col. 12, ln. 30-46).

Regarding claims 17 and 23, Sato discloses removing portion of the first insulating layer includes mechanical polishing separate from etching back (col. 6, ln. 52-57).

Regarding claim 18, Sato discloses that removing portions of the first insulating layer involves removing portions of the first insulating layer beyond portions of the raised pattern so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed relative to the exposed portions of the raised pattern (Fig. 4C, 9H).

Regarding claim 19, Sato discloses that a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern before removing portions of the first insulating layer (Fig. 4B, 9G).

Regarding claim 20, Sato discloses a substrate and a raised pattern on the substrate, forming a first insulating layer (12/6/7 in Fig. 4A-4H or 6/7/26/27 in Fig. 9A-9P) on the raised pattern and on the substrate such that a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern, after forming the first insulating layer, removing portions of the first insulating layer while maintaining portions of the first insulating layer so that the raised pattern extends beyond the maintained portions of the first insulating

layer and so that the maintained portions of the first insulating layer are recessed between portions of the raised pattern, and after removing portions of the first insulating layer, forming a second insulating layer (8 in Fig. 4A-4H and Fig. 9A-9P) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (Fig. 4A-4H and 9A-9P; col. 6, ln. 30 – col. 7, ln. 18; col. 11, ln. 45 – col. 13, ln. 48).

Claims 38, 46 and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (US 5,747,382).

Regarding claim 38, Huang discloses providing a substrate (10) having patterns (14A/14/14B) formed thereon, forming a first insulation layer (20) that has an level surface and covers the patterns by forming a first insulation material on the substrate, wherein voids (22) are formed at portions of the first insulation layer between the patterns, forming first insulation layer patterns between the patterns by etching the first insulation layer using an etch back process, wherein the first insulation layer patterns include widely opened voids, and forming a second insulation layer (30) having a level surface on the first insulation layer patterns by forming a second insulation material, wherein the second insulation layer fills up the opened void and covers the patterns (col. 3, ln. 49 – col. 4, ln. 25).

Regarding claim 46, Huang discloses that the voids have elliptical shapes and are positioned between the patterns (Fig. 1).

Regarding claim 47, Huang discloses etching the first insulation layer using a dry etch (RIE) process (col. 4, ln. 1-3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. (US 6,798,038) in view of Lee et al. (US 6,348,375).

Regarding claim 4, Sato discloses that the patterns can be metallization interconnection levels in an integrated circuit, but Sato does not specifically disclose that the patterns may be bit lines (col. 13, ln. 50 – col. 14, ln. 64). Like Sato, Lee discloses metallization interconnection patterns in an integrated circuit that have insulation material deposited over and therebetween. Lee discloses that the metallization may include bit lines, as is conventional in the art. At the time of the invention, it would have been obvious to one of ordinary skill in the art that the metallization levels of Sato include bit lines because Sato discloses that his invention is applicable to metallization interconnection levels in an integrated circuit and Lee shows that bit lines are examples of conventional metallization interconnections that are known in the art.

Claims 9-14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. (US 6,798,038) in view of Papasouliotis et al. (US 6,030,881).

Regarding claims 9, 10 and 21, Sato discloses forming the first portion (6/7) of the first insulating layer by using a HDP-CVD process and forming the second portion (26/27) of the first insulating layer by using a HDP-CVD process (col. 11, ln. 45 – col. 13, ln. 48). Sato does not specifically disclose the process conditions involved in these deposition processes. Like Sato,

Papasouliotis discloses using an HDP-CVD process to deposit oxide materials between features of an integrated circuit. Papasouliotis teaches that depositing the oxide layers using HDP-CVD involves determining the various deposition parameters according to the aspect ratio of the gap into which the oxide is deposited. Papasouliotis states, "Data from simulations and experiments can be used to maximize gap-fill process efficiency by varying the etch/dep ratio and deposition step duration according to specific wafer parameters prior to each deposition step. Methods to vary the etch/depth ratio are well-known in the art and include changing the chemical composition of the reactive gas mixture, the **power** supplied to the wafer, the **pressure** of the process chamber, and the temperature of the wafer." (emphasis added). Hence, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine appropriate chamber pressures and bias powers at which to deposit each of the layer of Sato because Papasouliotis states that optimizing these parameters is well-known in the art and such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claims 11-14, Papasouliotis discloses that oxide material can be successfully HDP-CVD deposited using a pressure of 1.5-25 mTorr, a bias power of 500-10000 kW, an oxygen gas flow rate of 10-1000 sccm, a helium gas flow rate of 10-1000 sccm and a silane gas flow rate of 10-250 sccm (Table 1).

Claims 9-14, 31-34, 41-45 and 49-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US 6,204,161) in view of Papasouliotis et al. (US 6,030,881).

Regarding claims 9, 10, 31 and 33, Chung discloses forming the first portion of the first insulating layer by depositing a thick oxide layer and forming the second portion of the first insulating layer by oxide depositing and sputtering using an HDP-CVD process (col. 7, ln. 52-59). Chung does not specifically disclose the process conditions involved in these deposition processes. Like Chung, Papasouliotis discloses using an HDP-CVD process to deposit oxide materials between features of an integrated circuit. Papasouliotis teaches that depositing the oxide layers using HDP-CVD involves determining the various deposition parameters according to the aspect ratio of the gap into which the oxide is deposited. Papasouliotis states, "Data from simulations and experiments can be used to maximize gap-fill process efficiency by varying the etch/dep ratio and deposition step duration according to specific wafer parameters prior to each deposition step. Methods to vary the etch/depth ratio are well-known in the art and include changing the chemical composition of the reactive gas mixture, the **power** supplied to the wafer, the **pressure** of the process chamber, and the temperature of the wafer." (emphasis added). Hence, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine appropriate chamber pressures and bias powers at which to deposit each of the layer of Chung because Papasouliotis states that optimizing these parameters is well-known in the art and such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claims 11-14, 32, 34 and 52-55, Papasouliotis discloses that oxide material can be successfully HDP-CVD deposited using a pressure of 1.5-25 mTorr, a bias power of 500-

10000 kW, an oxygen gas flow rate of 10-1000 sccm, a helium gas flow rate of 10-1000 sccm and a silane gas flow rate of 10-250 sccm (Table 1).

Regarding claim 41, Chung discloses forming the first insulation material on the substrate to cover the patterns by an HDP-CVD process under a first process condition, wherein the first insulation material has a maximum height over the patterns and has voids formed therein and a second insulation material having a level surface is formed on the first insulation material using a HDP-CVD process under a second processing condition. Like Chung, Papasouliotis discloses using an HDP-CVD process to deposit oxide materials between features of an integrated circuit. Papasouliotis teaches that depositing the oxide layers using HDP-CVD involves determining the various deposition parameters according to the aspect ratio of the gap into which the oxide is deposited. Papasouliotis states, "Data from simulations and experiments can be used to maximize gap-fill process efficiency by varying the etch/dep ratio and deposition step duration according to specific wafer parameters prior to each deposition step. Methods to vary the etch/depth ratio are well-known in the art and include changing the chemical composition of the reactive gas mixture, the **power** supplied to the wafer, the **pressure** of the process chamber, and the temperature of the wafer." (emphasis added). Hence, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine appropriate chamber pressures and bias powers at which to deposit each of the layer of Chung because Papasouliotis states that optimizing these parameters is well-known in the art and such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claims 42-45, Papasouliotis discloses that insulation material can be HDP-CVD deposited using a pressure of 1.5-25 mTorr, a bias power of 500-10000 kW, an oxygen gas flow rate of 10-1000 sccm, a helium gas flow rate of 10-1000 sccm and a silane gas flow rate of 10-250 sccm (Table 1).

Regarding claim 49, Chung discloses providing a substrate having conductive patterns formed thereon, forming a first insulation material (300) on the substrate to cover the conductive patterns by a HDP-CVD process under a first processing condition, wherein the first insulation material has a maximum height and has voids formed therein, forming a first insulation layer (300) having a level surface by forming a second insulation material (300) on the first insulation material under a second processing condition, forming first insulation layer patterns between the conductive patterns by etching the first insulation layer using an etch back process, wherein the first insulation layer patterns widely open the voids, and forming a second insulation layer on the first insulation layer patterns by forming a third insulation material (340/360), wherein the second insulation layer fills up the opened void and covers the conductive patterns (col. 7, ln. 38 – col. 8, ln. 36). Chung discloses forming the first portion of the first insulating layer by depositing a thick oxide layer and forming the second portion of the first insulating layer by oxide depositing and sputtering using an HDP-CVD process (col. 7, ln. 52-59). Chung does not specifically disclose the process conditions involved in these deposition processes. Like Chung, Papasouliotis discloses using an HDP-CVD process to deposit oxide materials between features of an integrated circuit. Papasouliotis teaches that depositing the oxide layers using HDP-CVD involves determining the various deposition parameters according to the aspect ratio of the gap into which the oxide is deposited. Papasouliotis states, "Data from simulations and experiments

can be used to maximize gap-fill process efficiency by varying the etch/dep ratio and deposition step duration according to specific wafer parameters prior to each deposition step. Methods to vary the etch/depth ratio are well-known in the art and include changing the chemical composition of the reactive gas mixture, the **power** supplied to the wafer, the **pressure** of the process chamber, and the temperature of the wafer." (emphasis added). Hence, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine appropriate chamber pressures and bias powers at which to deposit each of the layer of Chung because Papasouliotis states that optimizing these parameters is well-known in the art and such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claim 50, Chung discloses that each of the conductive patterns can include a gate structure formed on the substrate.

Regarding claim 51, Chung discloses that the first and second insulation materials are made of HDP oxides.

Regarding claim 56, Chung discloses that the voids are positioned between the conductive patterns and the voids have a circular shape.

Regarding claim 57, Chung discloses that etching the first insulation layer is performed by a wet etch process or a dry etch process (col. 8, ln. 16-18).

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 5,747,382) in view of Lee et al. (US 6,348,375).

Regarding claim 39, Huang discloses that the patterns can be any metallization interconnection levels in an integrated circuit, but Huang does not specifically disclose that the patterns may be bit lines (col. 5, ln. 9-14). Like Huang, Lee discloses metallization interconnection patterns in an integrated circuit that have insulation material deposited over and therebetween. Lee discloses that the metallization may include bit lines, as is conventional in the art. At the time of the invention, it would have been obvious to one of ordinary skill in the art that the metallization levels of Huang include bit lines because Huang discloses that his invention is applicable to any metallization interconnection levels in an integrated circuit and Lee shows that bit lines are examples of conventional metallization interconnections that are known in the art.

Claims 40-45 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US 5,747,382) in view of Papasouliotis et al. (US 6,030,881).

Regarding claims 40 and 48, Huang discloses that the first insulation material and second insulation material are deposited by PECVD processes (claims 5 and 9). Huang does not specifically disclose using an HDP-CVD process to deposit the first and second insulation materials. Like Huang, Papasouliotis discloses a method of depositing insulation materials between features of an integrated circuit. Papasouliotis teaches that it is beneficial to use HDP-CVD to fill narrow regions between features because the HDP-CVD process allows formation of void-free filling of narrow gaps that cannot be achieved by PECVD methods (col. 2, ln. 11-65). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a HDP-CVD process to deposit the insulation materials of Huang because Huang discloses filling gaps between features with the insulation material and Papasouliotis teaches that it is

advantageous to use HDP-CVD when attempting to fill narrow gaps because the HDP-CVD process allows formation of void-free filling of narrow gaps that cannot be achieved by PECVD methods.

Regarding claim 41, Huang discloses that the first insulation material has a maximum height over the patterns and has voids formed therein and a second insulation material is formed on the first insulation material. Papasouliotis discloses that the HDP-CVD process involves using a specified pressure and bias power (col. 6, ln. 40-65).

Regarding claims 42-45, Papasouliotis discloses that insulation material can be HDP-CVD deposited using a pressure of 1.5-25 mTorr, a bias power of 500-10000 kW, an oxygen gas flow rate of 10-1000 sccm, a helium gas flow rate of 10-1000 sccm and a silane gas flow rate of 10-250 sccm (Table 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
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